## DETAILED ACTION

### Request Continuation Examination

The request filed on 5/6/2008 for a Request Continuation Examination (RCE) under 37 CFR 1.53(d) based on parent Application No. 10/624,340 is acceptable and a RCE has been established. An action on the RCE follows.

### *Information Disclosure Statement*

The information disclosure statement (IDS) submitted on 5/6/2002 was filed after the mailing date of the notice of allowability on 2/5/2008. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### *Allowable Subject Matter*

Claims 1, 5-41, 52, 55-63, and 71-78 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claims 1,5, 8-11, 52, 55, 57-58, 71-72 and 75-76 the prior art alone or in combination does not teach the limitation of a capacitor construction comprising a conductive nitride layer between a first electrode being in conductive contact with the nitride layer, and a second electrode over the capacitor dielectric, the capacitor construction exhibiting a lower RC time constant compared to an otherwise identical capacitor construction lacking the conductive nitride layer.

With respect to claims 6,7,12, and 56, the prior art alone or in combination does not teach the limitation of a capacitor construction comprising an insulative nitride layer

between a first electrode and a surface supporting the capacitor construction, a capacitor dielectric over the first electrode.

With respect to claims 13-23, the prior art alone or in combination does not teach the limitation of a capacitor construction comprising: a rough silicon layer, a nitride layer under the rough silicon layer, a capacitor dielectric over the rough silicon layer.

With respect to claims 24-33, the prior art alone or in combination does not teach the limitation of a capacitor construction comprising: a conductive rough silicon layer over a support surface, a nitride layer between the rough silicon layer and the support surface, a first electrode comprising the rough silicon layer.

With respect to claims 34-41, the prior art alone or in combination does not teach the limitation of a capacitor construction comprising: a composite first electrode comprising a first conductive layer over and in conductive contact with the storage node and comprising a conductive polysilicon layer over and in conductive contact with the first conductive layer, the first conductive layer exhibiting a first conductivity greater than a second conductivity of the polysilicon layer.

With respect to claims 59-63, the prior art alone or in combination does not teach the limitation of a capacitor construction forming method comprising: forming a conductive polysilicon layer over and in conductive contact with the first conductive layer, the first conductive layer exhibiting a first conductivity greater than a second conductivity of the polysilicon layer and the first conductive layer and polysilicon layer being comprised by a composite first electrode.

With respect to claims 73-74 and 77-78, the prior art alone or in combination does not teach the limitation of a memory device comprising: a composite first electrode comprising a first conductive layer over and in conductive contact with the storage node and a conductive polysilicon layer over and in conductive contact with the first conductive layer, the first conductive layer exhibiting a first conductivity greater than a second conductivity of the polysilicon layer.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NGUYEN T. HA whose telephone number is (571)272-1974. The examiner can normally be reached on Monday-Friday from 8:30AM to 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diego F. Gutierrez can be reached on 571-272-2245. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nguyen T Ha/
Primary Examiner, Art Unit 2831